REMARKS

Claims 1-42 are pending in this application.

Claims 22 and 35 have been amended above, as requested by the Examiner in the office action at page 2, paragraphs 1-2. Other claim amendments are discussed below.

At page 2, paragraph 4 of the office action, claims 1-29 have been rejected under 35 U.S.C. 112, second paragraph as being indefinite.

The Examiner quotes the phrase "said portion" in Claims 1 and 18 and objects that there is insufficient antecedent basis. In response, Applicant points out that "said portion" in Claims 1 and 18 quite clearly refers to "a portion of said optical signal" in the previous line of the same claim. To advance prosecution, and without agreeing with the Examiner as to the alleged lack of antecedent basis, the objected-to language has been removed from Claims 1 and 18. The meaning remains the same.

The Examiner quotes the "said integrated circuit chip" in Claim 23 and objects that there is insufficient antecedent basis. Above, the claim has been rewritten withou the objected-to phrase.

Wherefore, reconsideration and withdrawal of the indefiniteness rejection are respectfully requested.

At page 3 of the office action, Claims 1-42 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Rao (US Patent No. 5,889,903) in view of Shanley (US Patent No. 6,477,285). The Examiner admits that Rao fails to teach a first semiconductor layer on a second semiconductor of a second semiconducting material, the first semiconducting material having a higher absorption coefficient than the second semiconducting material when both the first and second semiconducting materials are undoped. (Office action, page 4) Also, the Examiner admits that Rao fails to teach forming a device in the semiconductor layer to collect carriers generated by the optical signal.

Applicant respectfully traverses the obviousness rejection.

Clock skew is the difference in arrival times of clock edges to different parts of a chip. Most conventional digital logic requires precise clocking, and ideal synchronous

logic relies on clock signals arriving simultaneously to all.[1] There have been various attempts to solve a clock skew problem in computer systems and integrated circuits. Rao describes a method and apparatus for distributing an optical clock in an integrated circuit that eliminates clock skew by transmitting an infrared clocking pulse directed at the back surface of a Control Collapse Chip Connection (C4), flip chip, packaged chip. Silicon is partially transparent to infrared, so the optical clocking pulse penetrates through the silicon and is focused into P-N junction diode receivers at the front surface of the integrated circuit. The P-N junction diodes provide the electrical signals for local clocking. In Rao, the transparency of silicon is used and the optical clocking pulse is split and focused into a number of similarly configured P-N junctions distributed throughout the chip to provide local clocking so that clock skew is extremely small.[2] As Rao points out, only 1-2% of the photons are transmitted through a substrate that is approximately 720 μm thick. Rao addresses this problem by locally thinning the bulk silicon extending over the P-N junction receivers.[3] Another problem with directing light through the substrate, as described by Rao, is that the electrical conversion of the clocking signal may be blurred if the light passes through a substantial thickness of substrate. Light absorbed in the substrate generates minority carriers that have long lifetimes. The minority carriers in the Rao system persist for orders of magnitude longer than the clocking signal. The P-N junctions in Rao gradually collect these minority carriers, providing a background noise signal that decreases the signal to noise ratio of the clocking signal. This is particularly a problem if only 1-2% of the optical signal penetrates through the substrate to thin heavily doped regions.[4]

A person of ordinary skill in the art at the time of Applicant's invention recognized that Rao was uniquely suited to C4 packaging where the back side of the integrated circuit is exposed. Rao uses front side C4s for connections and avoids

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[1]Applicant's specification, Background, page 1, lines 11-15.

[2]*Id.*, page 2, lines 14-22

[3]*Id.*, page 2, lines 25-29.

[4]A *Id.*, page 3, lines 1-9.

shadowing clock signal reception by directing the clocking signal reception by directing the clocking signal to the back side of the integrated circuit and through the chip to receivers on the front side. A person of ordinary skill in the art appreciated that Rao had accomplished much for improving clock skewing in C4 packaging, and that Rao's structure balanced complicated competing concerns. Such a person would think that modifying Rao's structure or materials would be an extremely tricky matter.

The presently claimed invention provides unexpectedly superior results over Rao, by more effectively providing synchronized optical clocking signals to a plurality of circuit components on a silicon substrate with minimal signal degradation and a better signal to noise ratio while continuing to avoid shadowing from metal interconnect layers on the front surface of the chip so as to minimize or eliminate clock skew.

Applicant's present invention clearly is much beyond what a person of ordinary skill in the art could have accomplished. The differences between Rao and the presently claimed invention are more significant than the Examiner has given credit. The elegance and apparent simplicity now that the Examiner know Applicant's invention should not be confused with what a person of ordinary skill in Applicant's art at the time of the invention could have known and accomplished.

A person of ordinary skill in the art would not have been motivated to modify Rao as the Examiner has proposed. Rao is using only semiconductor **513**. Rao has nothing special to say about the semiconductor **513**. Rao fails to disclose any significance to be paid to the absorption coefficient of semiconductor **513**.

Shanley would not give the person of ordinary skill in Applicant's art motivation to modify Rao. Rao was particularly suitable to C4 packaging technology and particularly concerned with optical clocks. To the contrary, Shanley was otherwise. Moreover, Shanley's mention of clock skewing should not be given undue attention, keeping in mind that clock skew is a widely mentioned issue, appearing, for example, in over 2,100 U.S. patents.

The Examiner has artificially picked out a few parts of Shanley that the Examiner targeted because Rao was missing such features. However, a person of ordinary skill in Applicant's art would not read Shanley so selectively and would not take from Shanley what the Examiner argues. First, referring to Shanley's Background section, Shanley was

dealing with integrated circuit architectures that require certain signals to be supplied to many circuits. "For example, many circuits may need to receive the same clock or control signals. Similarly, many circuits may need to receive the same data signals." (Shanley, col. 1, lines 23-24.) That is, Shanley contemplated a variety of signals, not just clock signals.

Shanley's Background continues: "As integrated circuits become larger and denser, signal routing becomes more difficult, causing more valuable integrated circuit area to be used for routing data busses and global clock and control lines." (Id., lines 28-31.) As Shanley recognized, at the same time, performance demands are increasing. And, large integrated circuits have long and complex signal paths with signals routed through multiple wiring planes. (Id., lines 32-35.) The long complex paths increase signal propagation delay, and rapid propagation rates are needed. Shanley then recognizes that long complex clock lines can result in clock skewing problems. (Id., lines 45+). "To reduce or eliminate clock skew, long complex clock lines usually need additional circuitry to re-synchronize the phasing of the clock signal. Alternatively, a more complex system design can be used to compensate for the clock skew. Such a system design may involve, for example, circuitry to delay the signals or some portions of the circuit, thereby slowing overall operations. In either case, additional integrated circuitry is needed to support the additional clock circuitry, which further increases power consumption on the integrated circuit." (Id., lines 48-58.)

Shanley concludes his Background section by pointing out that "a need exists for large dense integrated circuits that have additional global wiring paths not requiring additional integrated circuit area. A need also exists for rapid data, clock, and control signal propagation; reduced power dissipation; and clock signals with little or no skew." (Shanley, col. 1, lines 59-63.)

Shanley invented certain "composite semiconductor structures" or "composite integrated circuits", such as a silicon-based CMOS device combined with a GaAs device. (Shanley, col. 2, lines 55-64.) Shanley particularly teaches a structure including a layer **26** of a monocrystalline compound semiconductor material. (Col. 1, line 11.) On the material side, it was monocrystallinity on which Shanley was focusing.

On the structural side, it was optical busses on which Shanley was focusing, namely, optical busses that can replace significant portions of conventional metal wiring. Shanley's structures significantly differed from those of Rao, so that there was no easy way to practically access benefits of Shanley.

A person of ordinary skill in the art would not combine Rao and Shanley. It would be too complicated for such a person of ordinary skill to try to balance Rao's considerations particular to clock skew in C4 packaging, and Shanley's provision of novel integrated circuits, with many details involving other aspects besides clock signals and clock skew. There is nothing about Shanley which naturally makes a person of ordinary skill, reading Shanley objectively from start to finish, want to modify Rao.

When the person of ordinary skill in the art reaches Shanley's passages cited by the Examiner, such as at col. 19, it must be remembered that he also is occupied with what he has been reading throughout Shanley. Moreover, he is reading all of Shanley without the special guidance that the Examiner now has (but must ignore) by virtue of Applicant's claims. Shanley calls for that person of ordinary skill in the art to focus on crystallinity (materials) and optical busses (structures).

In Shanley's Example 1 (col. 5-6), there is a monocrystalline silicon substrate **22**, a buffer layer **24** which is monocrystalline Sr-Ba-TiO_3, and an amorphous silicon oxide intermediate layer **28**. The buffer layer **24** is preferably about 10 nm thick, and is thick enough to isolate compound semiconductor layer **26** from substrate **22**. Thus, a particular structure is constructed in Shanley's Example 1, and where the semiconductor layer **26** is used in Shanley is unlike where the semiconductor **513** is used in Rao. The compound semiconductor layer **26** in Shanley's Example 1 is GaAs or AlGaAs. In Rao's structure, the silicon is important because it is partially transparent to infrared. Thus, clearly Shanley would not be feasible to apply to Rao because Shanley's silicon-free layers simply would not be thought useable in Rao where silicon's transparency to infrared is needed.

The same remarks apply to Shanley's other Examples. The basic structures in Shanley's Examples are not relatable to the structures in Rao. The structures in Shanley are not feasible for exploiting the transparency of silicon to infrared as is needed in the structure of Rao. For simplicity, the intervening Examples in Shanley are not all

discussed. However, clearly a person of ordinary skill in Applicant's art would see that those Examples of Shanley involve non-silicon materials and would never think of them as appropriate for combination with Rao.

In Shanley, col. 19 which the Examiner cites, Shanley teaches to use a "monocrystalline Group IV semiconductor layer **174**" that "includes germanium, silicon germanium, silicon germanium carbide, or the like." (Col. 19, lines 4-7.) However, no one of ordinary skill in Applicant's art would want to use a non-silicon containing layer, namely, germanium, Rao's first mentioned example, in the Rao structure, because he would assume that the absence of silicon in the layer would mean that the desired infrared-transparency could not be provided. The person of ordinary skill in the art would naturally treat what Shanley is doing and what Rao is doing as separate, because there would be no sensible way to mix the principles from the two references in the mind of a reader of ordinary skill in Applicant's art.

Additionally, a person of ordinary skill in the art cannot reasonably be assumed to want to make Rao's structure more complicated (whether by adding another material or another layer or otherwise introducing more parts) unless a sound articulated reason exists. Usually, simplification, not additional complexity, is wanted.

For all those reasons, the Examiner's theory of combinability of Rao and Shanley is an improper assumption.

Moreover, even with Rao and Shanley, a person of ordinary skill in Applicant's art would not arrive at Applicant's presently claimed invention. Shanley emphasizes monocrystallinity in composite semiconductors. Neither Shanley nor Rao even mention absorption coefficients as recited in Applicant's presently claimed invention. Also, Rao and Shanley's structures are too different from each other.

Reconsideration and withdrawal of the obviousness rejection are respectfully requested.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1-42 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone

number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees for the petition or for entry of this amendment to Attorney's Deposit Account No. 09-0458 (IBM Fishkill).

Respectfully submitted,

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